Akshad Dhamande

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PROFESSIONAL SUMMARY

Electronics and Communication Engineering graduate with hands-on experience in digital and analog VLSI design, semiconductor fabrication, and FPGA implementation. Proficient in Cadence Virtuoso, Verilog HDL, and semiconductor characterization techniques. Skilled in hardware validation, circuit testing, and debugging with a strong interest in semiconductor technologies and electronic systems.

TECHNICAL TRAINING

Digital Design and VLSI using Verilog | Shri Vaishnav Vidyapeeth Vishwavidyalaya June 2025 – July 2025

- Participated in technical training on Semiconductor Fabrication and Characterization.
- Studied semiconductor fabrication processes, including photolithography, etching, and metallization.
- Performed cleanroom demonstrations and characterization techniques for semiconductor devices.

Analog Chip Designing | Shri G. S. Institute of Technology & Science (SGSITS) Feb 2025 – Mar 2025

- Completed intensive hands-on training in Analog IC Design using Cadence Virtuoso.
- Designed and simulated OTA and Schmitt Trigger circuits.
- Performed schematic, layout, DRC/LVS, and post-layout verification.

TECHNICAL SKILLS

Expertise Areas: RTL Design, Analog Chip Designing, Digital Logic Design.
Software & EDA Tools: Cadence Virtuoso, Vivado, Quartus Prime, Open ROAD.
Core Skills: Semiconductor Fundamentals, Hardware Debugging, Root Cause Analysis, FPGA Implementation.
Programming Languages: Verilog HDL, System Verilog.
Protocols: UART, SPI, I²C

EDUCATION

Bachelor of Technology (B. Tech) – Electronics & Communication Engineering Nov 2022 – Jun 2026
Prestige Institute of Engineering Management & Research (PIEMR), Indore
CGPA: 7.2 / 10

PROJECTS

Design and Analysis of 6T, 8T, and 10T SRAM Cells in CMOS Technology using Cadence Feb 2026

- Designed 6T, 8T, and 10T SRAM cell schematics using Cadence Virtuoso.
- Developed layouts and performed DRC, LVS, and PEX verification.
- Simulated SRAM read/write/hold operations and analyzed SNM, power, delay, and area.
- **Tools/Skills:** SRAM Design & Analysis, DRC, LVS, Cadence Virtuoso.

Implementation and Verification of OTA & Schmitt Trigger Mar 2025

- Designed and simulated OTA and Schmitt Trigger circuits using Cadence Virtuoso.
- Performed schematic design, layout, and simulation for OTA and Schmitt Trigger circuits.
- Gained hands-on experience in analog circuit design and verification.
- **Tools/Skills:** Cadence Virtuoso, Analog CMOS Design, AC Analysis, Layout Design, DRC, LVS, PEX, GDSII.

PS/2 Keyboard Interfacing with FPGA July 2025

- Interfaced PS/2 keyboard with FPGA to display key inputs on a 7-segment display.
- Implemented basic Verilog design for data capture and display.
- Learned digital input handling and FSM design.
- **Result:** Displayed key inputs accurately on the 7-segment display during testing.

CERTIFICATES & TRAINING

- Analog Chip Design Internship – SGSITS (2025)
- Digital Design and VLSI using Verilog – SVVV (2025)

ACHIEVEMENTS

- Recognition in Urjotsav 2K25 Project Competition