Signaloid

4 Station Square
Cambridge CB1 2GE, UK.
T: +44 1223 856982
W: https://signaloid.com

FOR IMMEDIATE RELEASE

Signaloid announces preview of new ASIC targeted at physical AI and robotics applications

- *Signaloid previews a new ASIC purpose-built for physical AI and robotics workloads.*
- *The chip, taped out with TSMC in partnership with IC-Link by imec and Cadence, is projected to deliver up to 1000× better performance-per-watt in key physical AI workloads.*
- *Built on Signaloid's UxHw® technology, the ASIC complements the company's cloud platform and FPGA-based hardware modules, which already deliver major speedups for quantitative finance and engineering simulations.*

Cambridge UK, 2nd June 2026 — Signaloid (https://signaloid.com), a computing platform company providing hardware and binary-translation-based acceleration of AI, robotics, aerospace, and quantitative finance workloads, today announced the tapeout and preliminary specifications documents for its C0-ASIC. Delivery of engineering samples to the first customer is due in Q3 2026, and additional FPGA-based systems implementing the ASIC's register-transfer-level (RTL) design are under discussion for deployment in the UK and Switzerland later in 2026.

The new ASIC and the FPGA-based accelerators complement Signaloid's existing hardware starter modules (available through electronics distributor Mouser) and cloud-hosted implementations of its technology, already being used or evaluated in aerospace, quantitative finance, and high-performance physics simulations.

The C0-ASIC was targeted specifically at energy-efficient physical AI workloads. The UK Advanced Research and Invention Agency (ARIA) will take delivery of systems based on the ASIC for use in next-generation AI workloads such as second order methods.

"The Scaling Compute program at ARIA commissioned several innovative technology prototypes pursuing unconventional ideas to design new AI accelerators", says ARIA Program Director Suraj Bramhavar. "*We commissioned Signaloid's C0-ASIC for evaluation in randomized numerical linear algebra and probabilistic computing workloads. We believe randomized linear algebra represents a fundamentally new and powerful technique underpinning many applications in computer science including AI, and exploiting these principles in hardware could provide an entirely new vector for improved performance. We are excited to invest behind this theme, in partnership with Signaloid, to explore its full potential.*"

A Different Kind of AI Compute Accelerator

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The C0-ASIC implements Signaloid's distribution-extended compute hardware (UxHw®) technology.

Unlike conventional CPUs and GPUs, which use impressive amounts of sheer compute force across thousands of compute cores, to solve problems that require iterative randomized variations, Signaloid's UxHw builds on new mathematical techniques to restructure computations, dynamically, to achieve the same results while often using 1000-fold (or more) less energy.

Signaloid has already deployed implementations of UxHw using a combination of binary translation and FPGA-based hardware implementation, ahead of custom silicon availability. Implementations for robotics applications are available through Mouser, with demonstrated performance improvements of, e.g., over 37-fold for robotics particle filter algorithms. Implementations for large-scale workloads are available today through Amazon Web Services (AWS), and have demonstrated more than 580× speedup for Heath–Jarrow–Morton swaptions pricing, over 430× speedup for Value at Risk (VaR) on geometric Brownian motion processes, and over 80× acceleration for radiation transport simulations, compared with AWS r7iz instances.

The UxHw technology and its implementation is covered by a growing portfolio of over 90 intellectual property filings in the US, China, Taiwan, Japan, and the EU.

What the ASIC Will Enable

Signaloid's existing deployment of UxHw already provides multiple orders of magnitude speedup over the status quo. The C0-ASIC will permit even greater improvements in performance and energy-efficiency.

"The kinds of compute workloads that Signaloid's UxHw is designed for, pervade many aspects of robotics, physical AI, engineering, and quantitative finance," says Phillip Stanley-Marbell, founder and CEO of Signaloid. *"The C0-ASIC took the lessons we have learned from shipping our binary-translation-based and FPGA implementations of UxHw and making as efficient a silicon implementation as possible. The additional step-change in efficiency will make possible even more advanced algorithms like efficient probabilistic and Bayesian methods in robotics, which in turn could be the enabler of more adaptable and resilient physical AI."*

An International Partnership

The design and implementation were the result of a collaboration between Signaloid and world-leading design partners IC-Link by imec and US-based Cadence Design Systems.

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"Leading AI hardware innovators trust IC link as a key partner to bring their most advanced ASIC concepts through design and into production with our foundry partner TSMC," says Ozgur Gursoy, Director Portfolio & Strategy for IC-Link's ASIC services. *"We are proud to have partnered with Signaloid in bringing the C0 Dreadnought ASIC from concept through the design cycle, enabling a new class of compute efficiency for distribution-enhanced computing applications."*

Speaking of the partnership, John Heighton, sales group director, EMEA North and Central at Cadence, said, *"Cadence sets the industry standard for enabling leading companies to tape out cutting-edge AI silicon, including Signaloid's C0-Dreadnought, now in production at TSMC. We support startups advancing next-generation computing by delivering our high-performance Artisan SRAM memories for Signaloid's ASIC."*

Availability

Engineering samples of bumped dies of the C0-ASIC will be available in Q3 2026. A 2-page preliminary design brief of the C0-ASIC is available immediately, for qualifying customers. Customers interested in robotics and industrial automation use cases will also be able to see the UxHw technology in action at the Bosch Connected World flagship event in Berlin, from 10th-11th June 2026.

About Signaloid

Signaloid was founded by Prof. Phillip Stanley-Marbell, former Professor of Physical Computation at the University of Cambridge and a researcher whose previous roles include Bell Labs, IBM, Apple, and MIT. Signaloid provides a computing platform that benefits computationally-challenging workloads, many of which can be reformulated in terms of algorithms that process probability distributions. Its technology is already used by more than 3,000 users worldwide and is available as cloud, on-premises and low-power edge hardware. www.signaloid.com

Press contact: press@signaloid.com