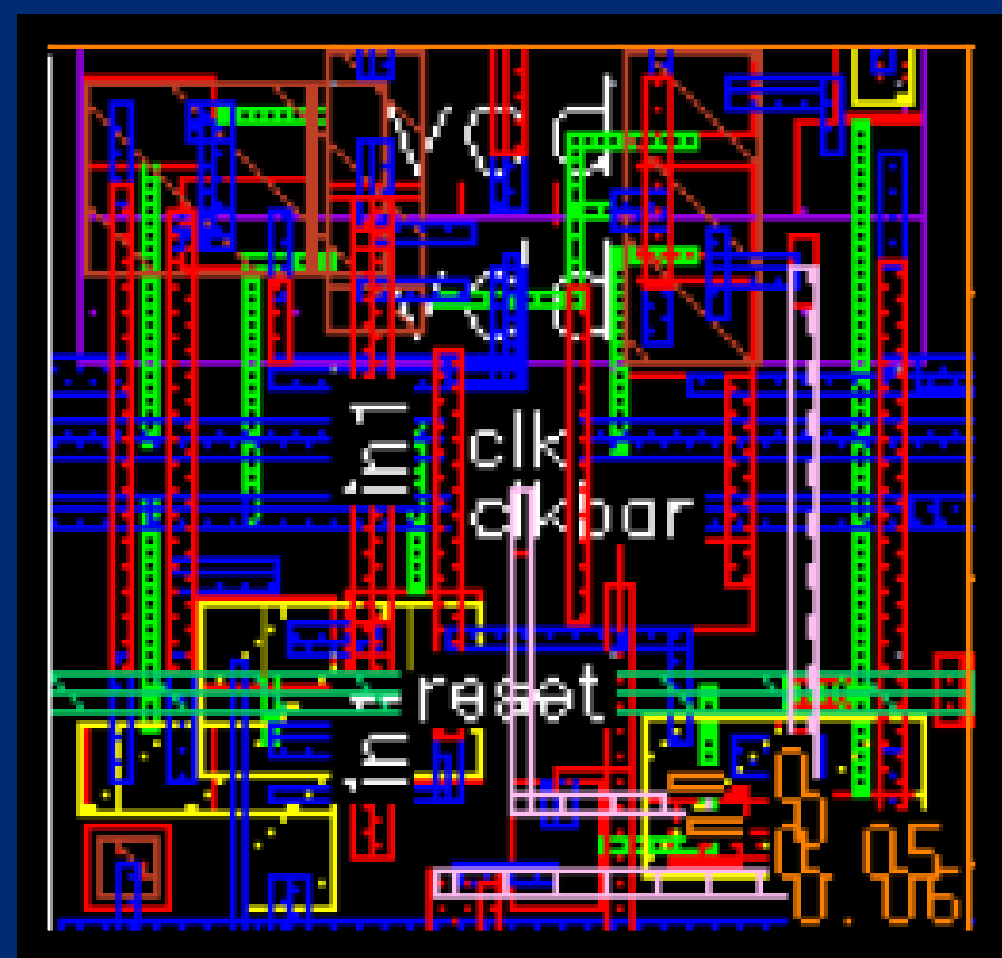




Low-Area CMOS Keyword Spotter

CMOS keyword spotting system for wake-word detection with layout-area-conscious design

Joseph Gregory, Gwenyth Tran, and Taiyo Tagami
EN.520.216.01.SP26, Introduction to VLSI - Dr. Ralph E. Cummings
Whiting School of Engineering, Johns Hopkins University



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WHITING SCHOOL
of ENGINEERING

THE CHALLENGE

Always-On Voice Detection at Low Power

Voice assistants can be activated even when the device appears idle. Continuous speech processing would be too power-intensive, so systems may rely on a low-power CMOS-based keyword spotter to detect trigger phrases efficiently. It must be compact and energy-efficient to fit and perform well in the device.

OBJECTIVES

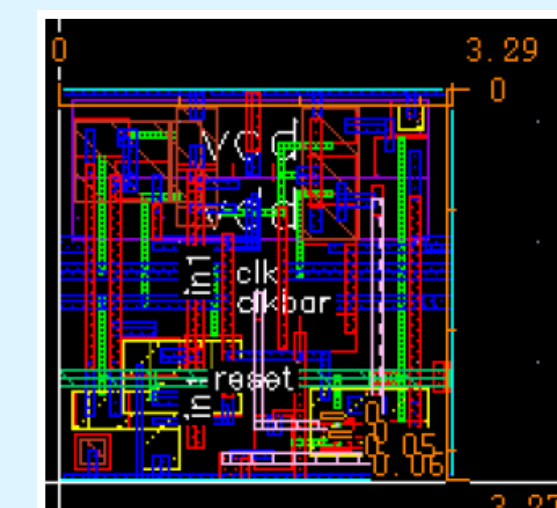
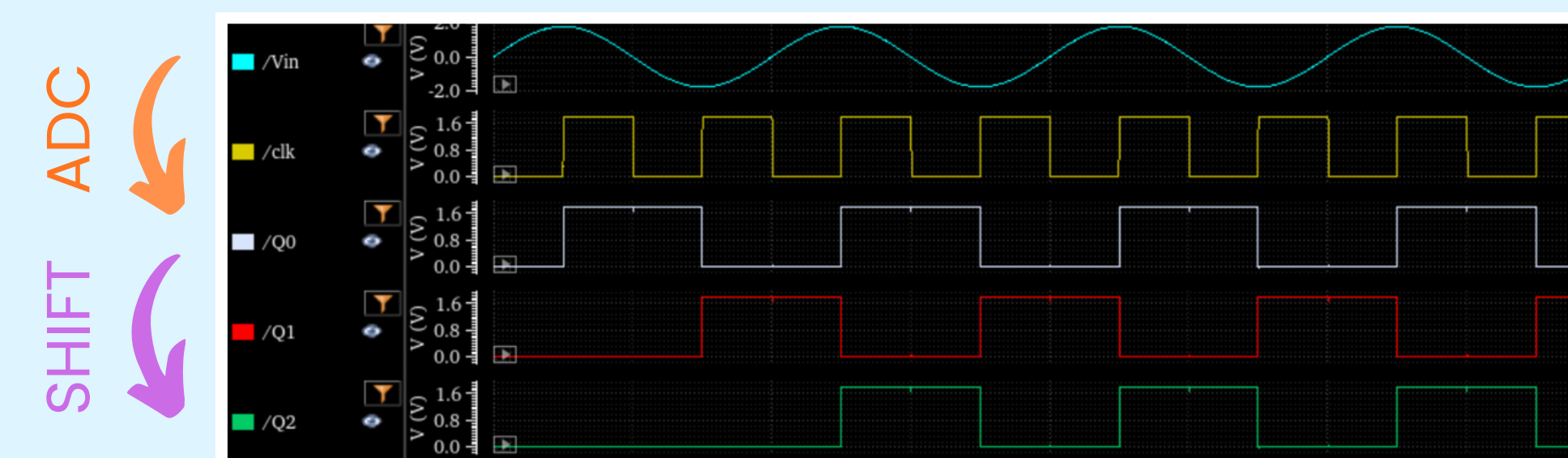
Design CMOS-based keyword spotter architecture
→
power efficiency and speed

RESULTS

A

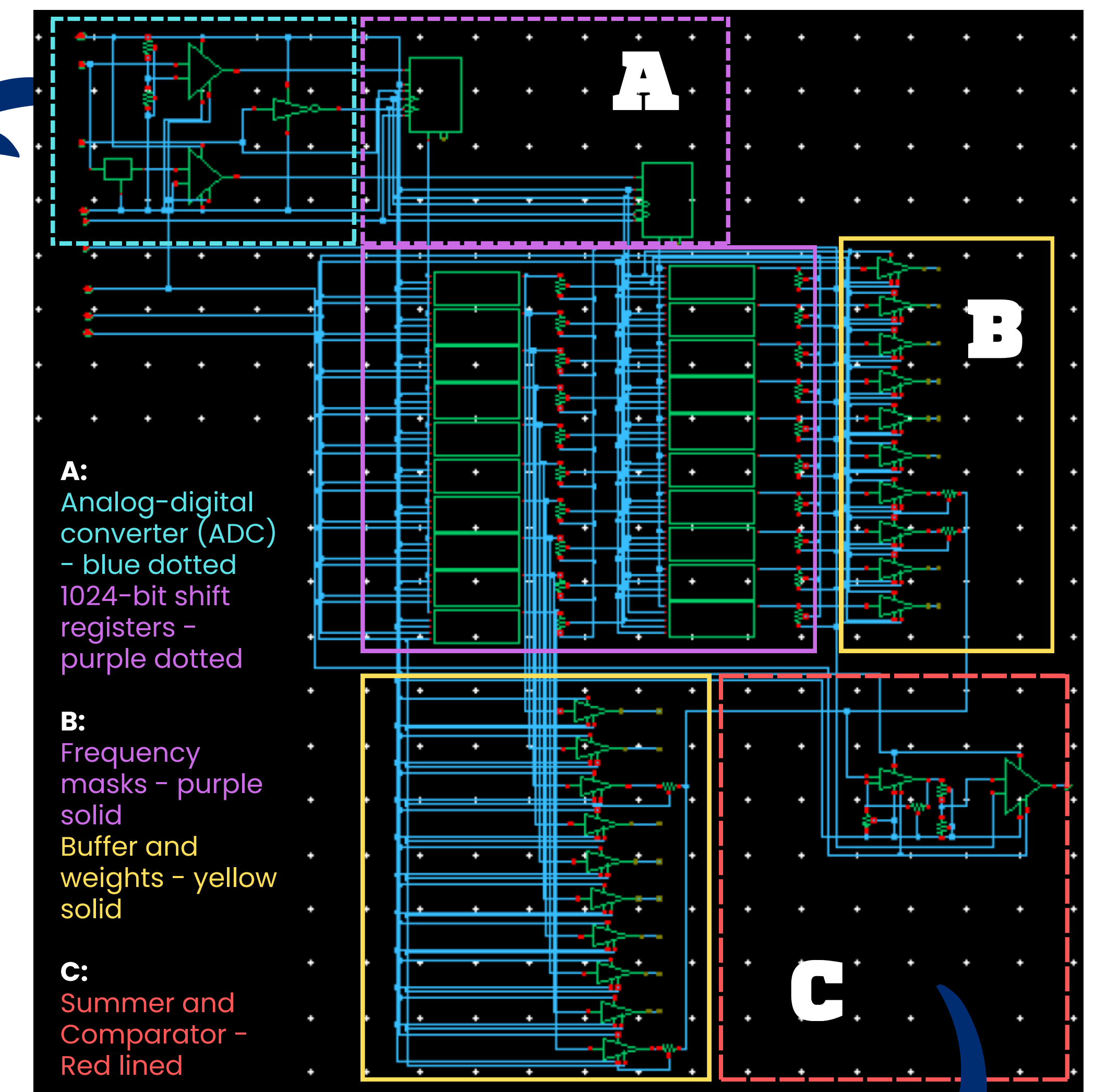
Input & Binary Encoding (ADC + Registers)

- High-pass filter designed with **pseudo resistor** differentiates input signal
- Comparators digitize raw signal in a process called analog-digital conversion (ADC) using thresholds: $v > \frac{V_{DD}}{2}, \frac{\partial v}{\partial t} > 0$
- Signals pass through and are stored in 1024-bit shift registers for ~1 second



Layout areas:

- Comparator: 2.305 x 2.520 μm^2
- D Flip-Flop: 3.290 x 3.275 μm^2
 - Aggregated for shift register
- High-pass: 7.670 x 1.405 μm^2



A: Analog-digital converter (ADC)
- blue dotted
1024-bit shift registers - purple dotted

B: Frequency masks - purple solid
Buffer and weights - yellow solid

C: Summer and Comparator - Red lined

C

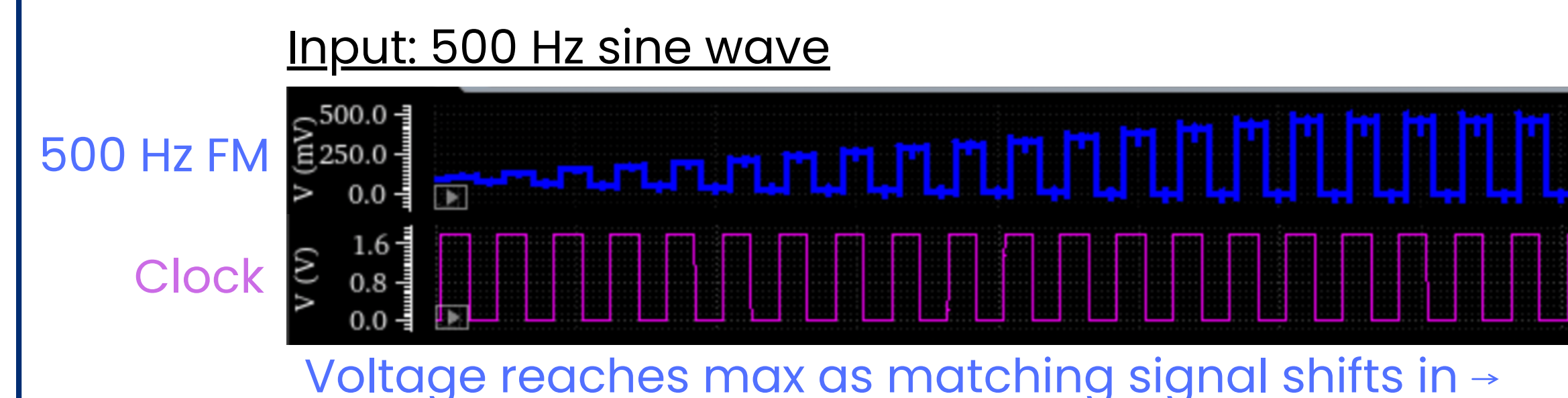
Perceptron and Output

- Implemented summer amplifier to sum weights
- Flagged wake-word detection using comparator

B

Current Source Array (Frequency Masks)

- Frequency masks detect given frequencies
- Op-Amp buffer** designed to separate masks and weight blocks

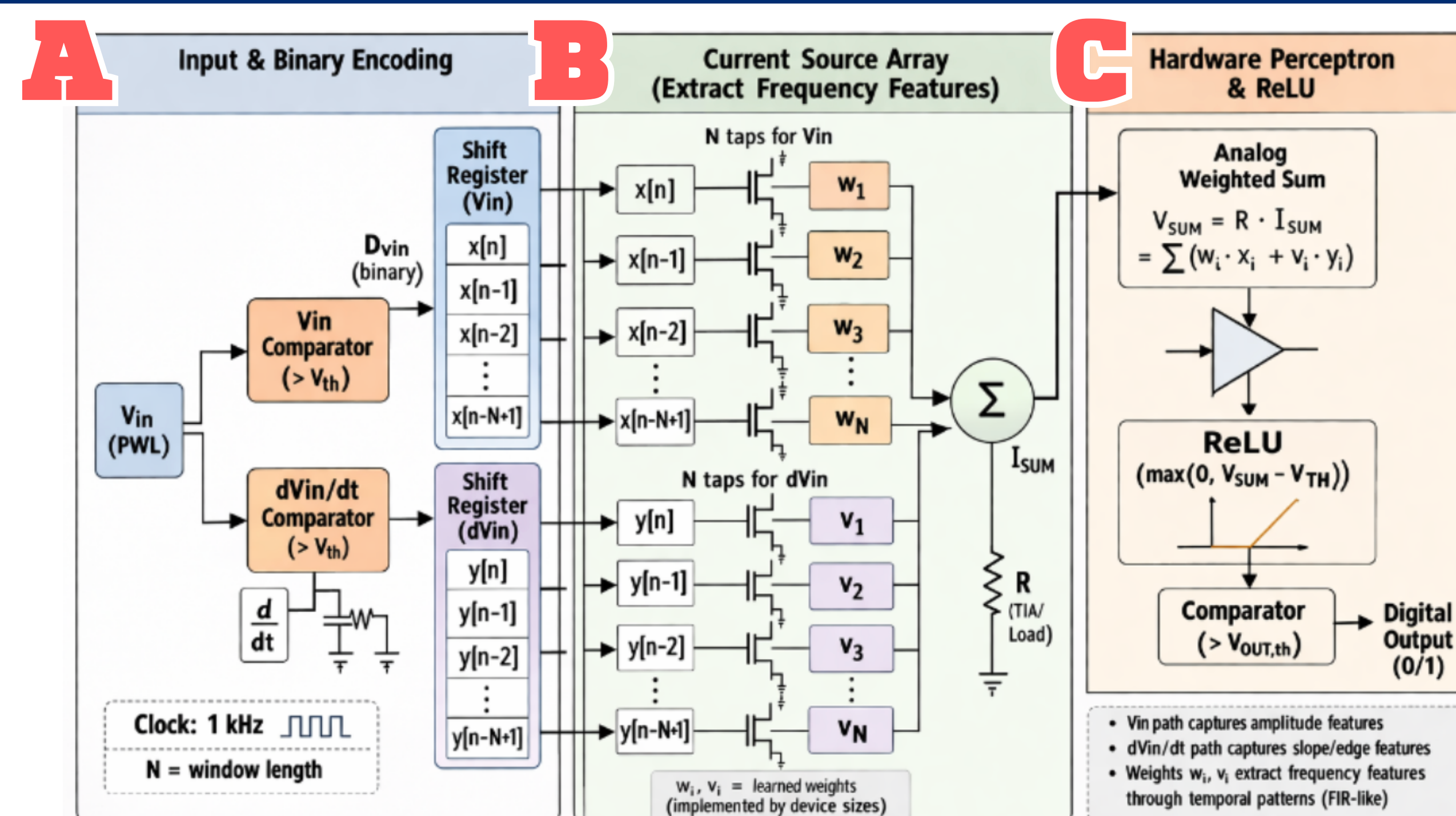


V

CONCLUSION

- A wake-word detector was successfully created in Cadence
- Experimented and researched designs that maintain compact layout area
- Layout was created for designed components

METHODS

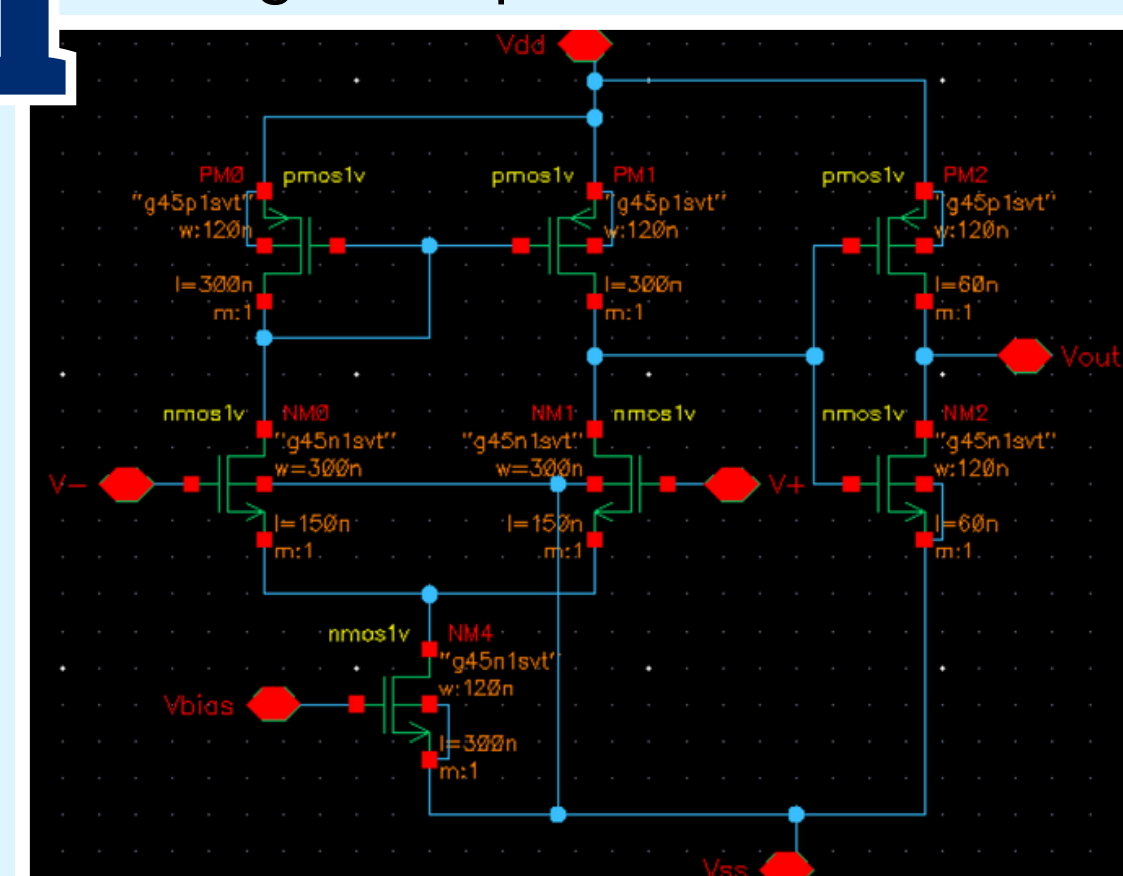


Keyword spotter design process. Adapted from Prof. Ralph E. Cummings, EN.520.216.01.SP26, 2026

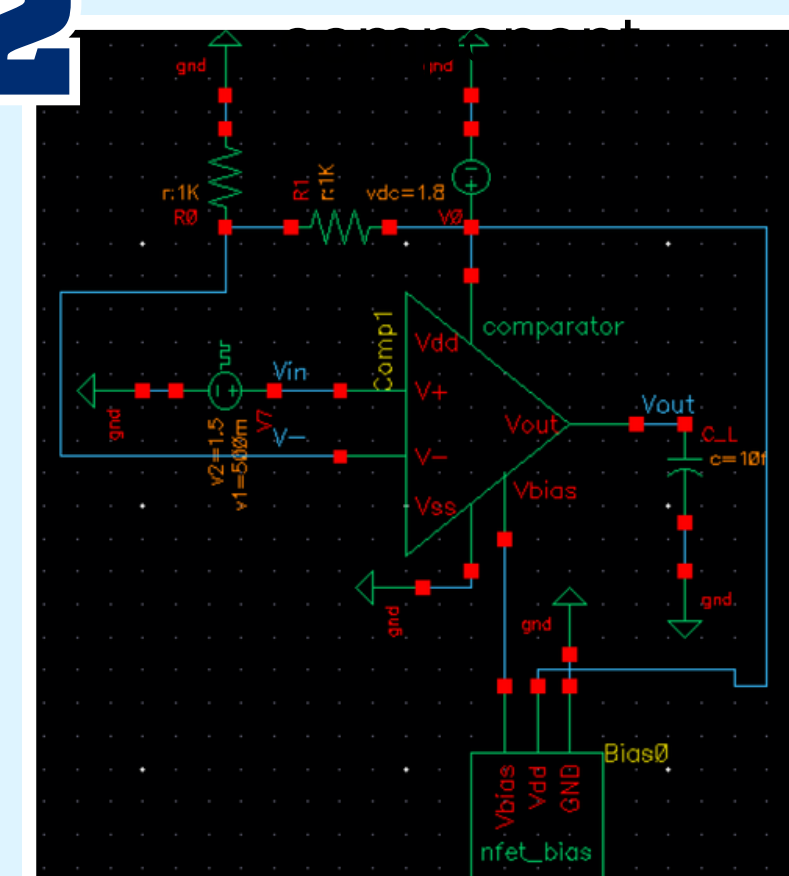
COMPONENT DESIGN PROCESS

*Diagrams below are for the comparator.

1 Design component schematic



2 Test and simulate



2D CAD Software: Cadence Virtuoso

Complete small layout, passing DRC and LVS

